Intel Corporation

Serial No.: 10/007,007 Docket No.: P12809

Remarks

The Official Action rejected claims 1-29. Applicant has added claims 30-37. Claims 1-37 remain pending. Applicant respectfully requests allowance of the pending claims in light of the points that follow.

Claim Rejections - 35 USC § 102

The Official Action rejected claims 1-6, 13-18, and 25-27 under 35 USC 102(b) as being anticipated by Watkins et al (US 5,220,512). Applicant respectfully requests the rejection of the pending claims to be withdrawn.

As is well-established, in order to successfully assert a prima facie case of anticipation, the Official Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Official Action has not succeeded in making a prima facie case.

Claims 1-6 and 13-18

Each of claims 1-6 and 13-18 require having the logic design element automatically collect instrumentation data during the simulation, wherein the instrumentation data relate to the logic design element.

The electronic computer aided design (ECAD) system (described in col.4, lines 52-56) of Watkins provides the characteristics of schematic editor, schematic compiler, and the simulator together as a single integrated function to a user. Watkins discloses (in col. 10, lines 53-63 describing Fig. 3) a display screen 300 to display the textual state information, at different points to be monitored, when provided with different input values. Also, Watkins discloses (in col. 11, lines 8-14,

Serial No.: 10/007,007

describing Fig. 4) a display screen 400 displaying timing diagrams, at different points to be monitored, when provided with different input values.

Watkins simply teaches an ECAD system to collect the results (textual or graphical) at different points to be monitored in the logic circuit after providing inputs to the logic circuit. The ECAD system comprises a schematic editor to provide inputs and observe the results and a simulator to perform simulation. The logic circuit may be simulated with commands representing a set of initial conditions or a simulation stepped run, which continues from the last simulation's ending point. Further, Watkins appears to teach a user adding state displays (e.g. 310, 312, 314) and state tables 318. In other words, Watkins appears to disclose a system which requires a user to add additional components (e.g. state displays, state tables) to a logic design in order to obtain state information about a particular logic design element or schematic component such as flip-flop 302. However, Watkins does not appear to teach having the schematic components 304, 306, and 308 collecting data about themselves as required by the logic design elements of the invention of claims 1-6 and 13-18. Watkins appears to delegate data collection or monitoring to state displays 310, 312, 214 and state tables 318 which are not part of the logic circuit.

Since Watkins does not teach having the **logic design element automatically collect instrumentation data during the simulation, wherein the instrumentation data relate to the logic design element**, Watkins does not anticipate the invention of claims 1-6 and 13-18. Applicants respectfully request the rejection of claims 1-6 and 13-18 be withdrawn.

Claims 25-27

Each of claims 25-27 requires a collection module that is integrated with the logic design element and that is structured and arranged to automatically

Intel Corporation Serial No.: 10/007,007

Docket No.: P12809

collect instrumentation data relating to the logic design element during the simulation.

As described above, the ECAD system of Watkins enable a user to provide commands to the simulator using a schematic editor and observe the results of simulation, corresponding to outputs at the points to be monitored, on the schematic editor. The ECAD system of Watkins does not teach a collection module that is integrated with the logic design element and that is structured and arranged to automatically collect instrumentation data relating to the logic design element during the simulation. Since, Watkins does not teach every limitation of claims 25-27, Watkins does not anticipate the invention of claims 25-27. Applicant respectfully requests the rejection of claims 25-27 be withdrawn.

Claim Rejections - 35 USC § 103(a) (Watkins/Sharma)

The Official Action further rejected claims 7-9, 19-21, and 28 under 35 USC 103(a) as being unpatentable over Watkins (US 5,220,512) in view of Sharma (US 5,978,574). Applicants respectfully request allowance of claims 7-9, 19-21, and 28 in light of the points that follow.

Claims 7-9, 19-21 and 28

The proposed combination of Watkins/Sharma is improper as a result of Sharma teaching away from the combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983).

Sharma discloses (in col. 1, lines 63-67) an aspect of queue flow control of a FIFO. Sharma indicates (in col. 2, lines 32-35) that emulations cover more cases than simulations and even emulation does not guarantee that all cases are verified in the various queues. Sharma, in fact, states (in col. 2, lines 14-16) that simulation is

Intel Corporation Serial No.: 10/007,007

Docket No.: P12809

problematic since it is very difficult to stress the queues enough to get to the corner cases. As a result, Sharma advocates a model checking approach that provides a formal verification of the design instead of simulation (col. 2, lines 14 through col. 3, line 56). In light of this teaching away from simulation techniques for queue verification by Sharma, one skilled in the art would have no motivation to combine the model checking teachings of Sharma with the simulator of Watkins in order to arrive at the proposed combination.

Since the proposed combination is in improper in light of Sharma teaching away from simulations, Applicant respectfully request the rejection of claims 7-9, 19-21 and 28 be withdrawn.

Claim Rejections - 35 USC § 103 (Watkins/Mitchel)

The Official Action further rejected claims 10-12, 22-24, and 29 under 35 USC 103(a) as being unpatentable over Watkins (US 5,220,512) in view of Mitchell (US 5,646,553). Each of claims 10-12, 22-24 and 29 depends from one of claims 1, 13 and 25. Accordingly, each of claims 10-12, 22-24 and 29 is allowable for at least the reasons given above in regard to claims 1, 13 and 25. Applicants respectfully request the rejection of claim 10-12, 22-24 and 29 be withdrawn.

13

Intel Corporation Serial No.: 10/007,007

Docket No.: P12809

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicants submit that the application is in condition for allowance.

Reconsideration is requested, and allowance of the pending claims is earnestly

solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or

1.17, or any excess fee has been received, please charge that fee or credit the

amount of overcharge to deposit account #02-2666. If the Examiner believes that

there are any informalities, which can be corrected by an Examiner's amendment, a

telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,

GregoryCD. Caldwell

Reg. No. 39,926

c/o Blakely, Sokoloff, Taylor & Zafman LLP 12400 Wilshire Blvd. Seventh Floor

Los Angeles, CA 90025-1030

408-720-8300

14